Digital Acquisition Board (DAB) for LHC Orbit System

- **People involved:**
  - **Jean-Jacques Savioz: FPGA**
  - **Rhodri Jones: Hardware responsible**
  - **Daniel Cocq: WBTN responsible**
  - **Lars Jensen: Software responsible**

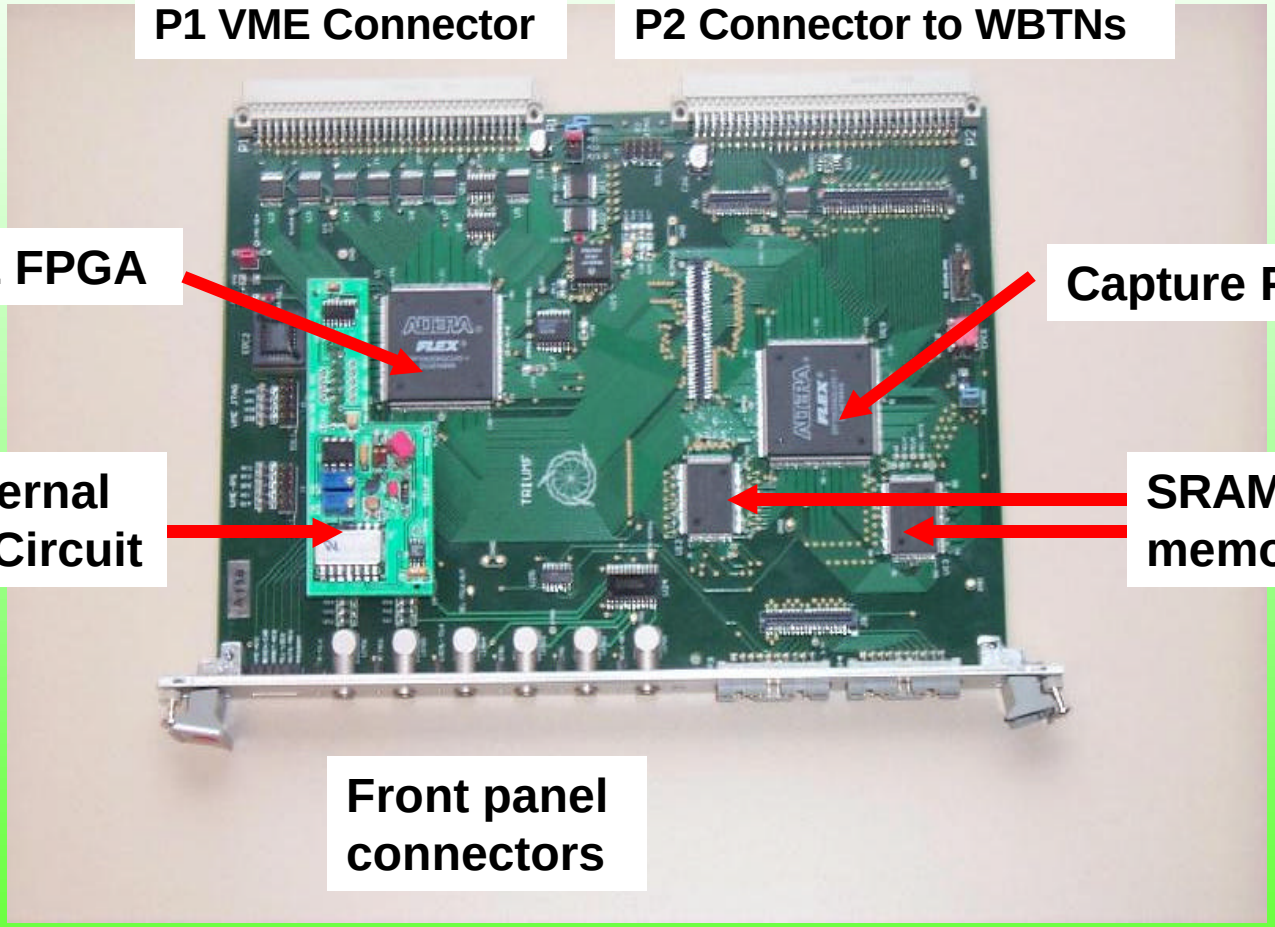
Outline

- The DAB module, developed with Triumf (Canada) allows beam measurements at 40 MHz
- Measurements in the lab (WBTN calibration pulses)
- Measurements on the beam
  - Calibration with MOPOS system
  - AC dipole studies
  - Electron Cloud
- Cabling problems to WBTN
- Radiation tests TCC2
- Future of the DAB module (SPS and LHC)
- Conclusions

The DAB VME prototype module

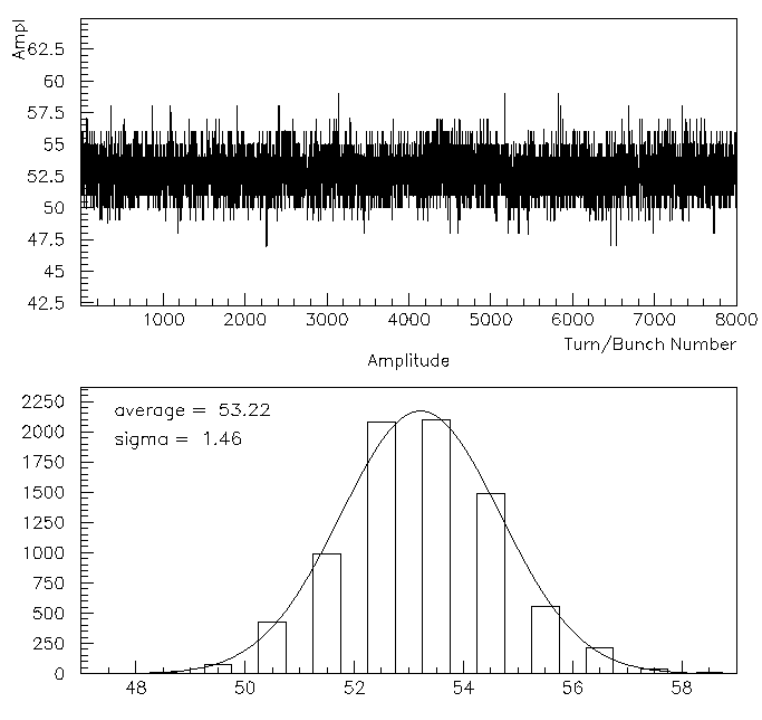
- 6U VME module
- Two Altera FPGAs for the logic
  - 1) VME accesses (A24D16, DMA, interrupt)
  - 2) Presently only ‘random’ (capture) acquisitions available
  - 3) Capture registers allow acquisitions of selected bunches over selected number of turns and storage in SRAM memory (max number of data (bunches*turns) = 2^16)
- PLL creates the 40 MHz clock (from SPS Frev) for the synchronised acquisition of Hor + Ver position (+ the intensity signal, not yet)
- Use of external 40 MHz timing to replace the PLL, is foreseen (TTC ?)
- Digital delay line (step ~ 2 [nsec]), to synchronise with WBTN (auto-trigger principle), where the ADC (10 bit unipolar) is placed.

The DAB module
The Big Picture



Measurements in the lab
Calibration with WBTN

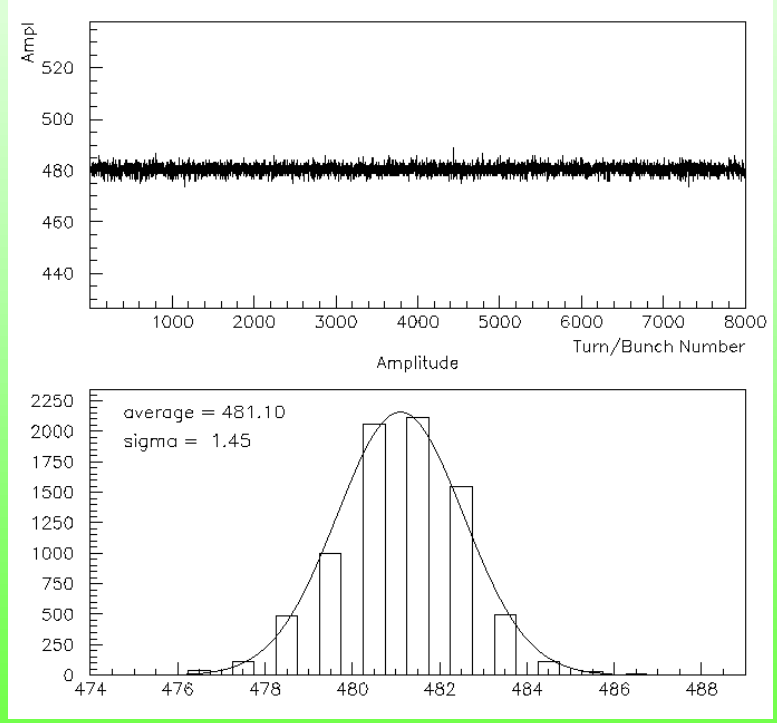
Calibration with ‘LEFT’ ADC value



ADC raw-data (bins)

Noise floor ~ 40 [um]

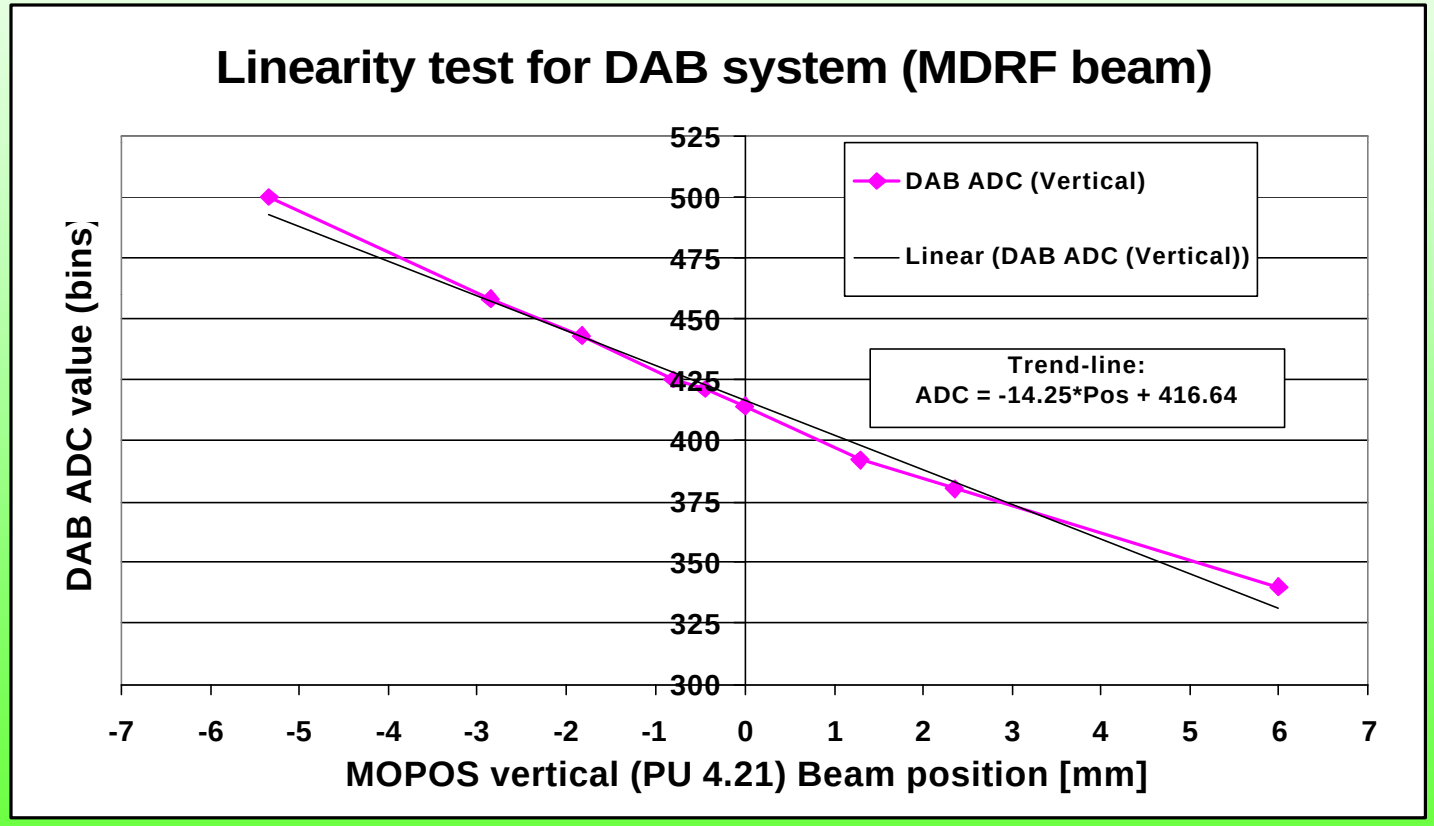
Calibration with ‘CENTRE’ ADC value



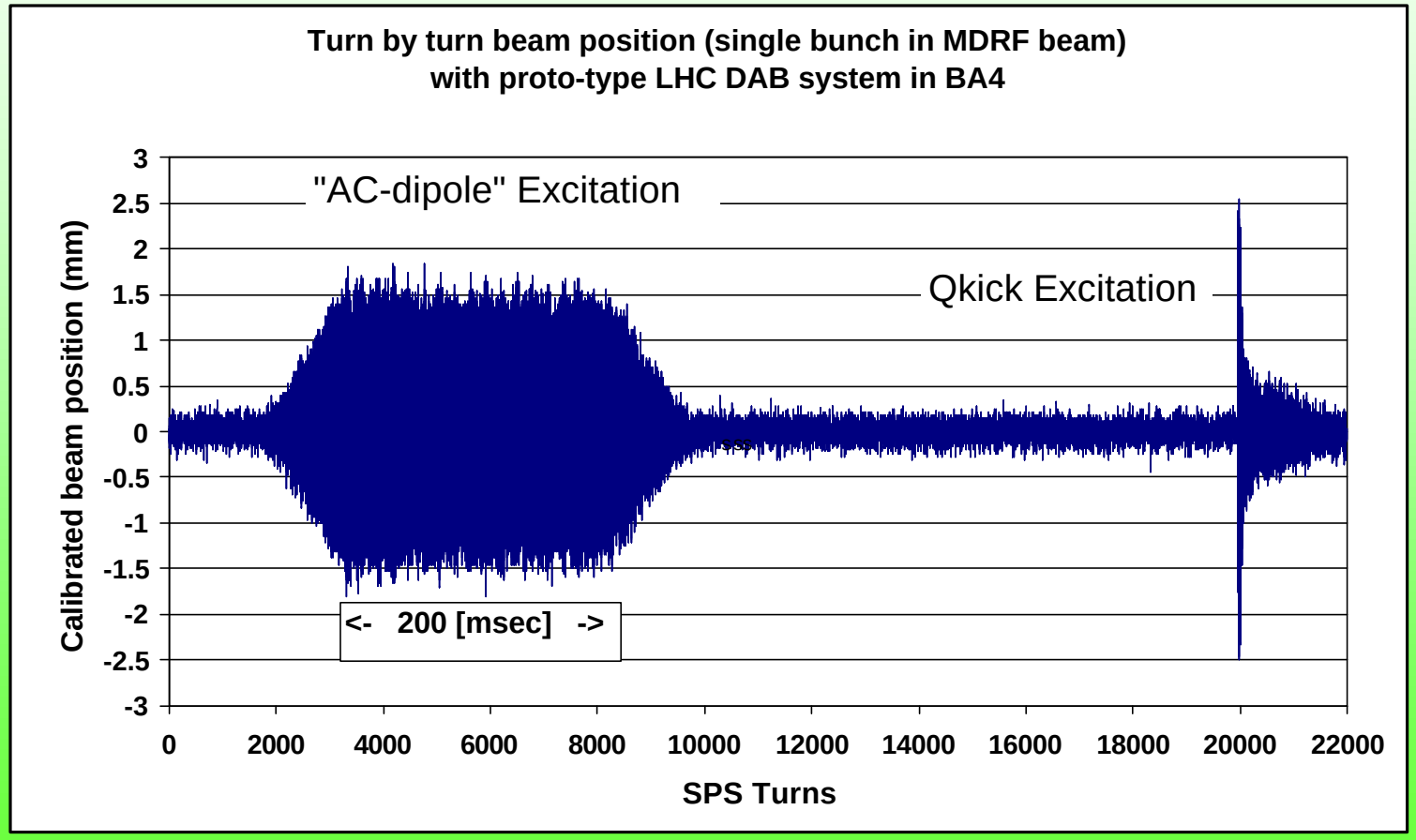
ADC raw-data (bins)

Measurements on the beam (Calibration with MOPOS)

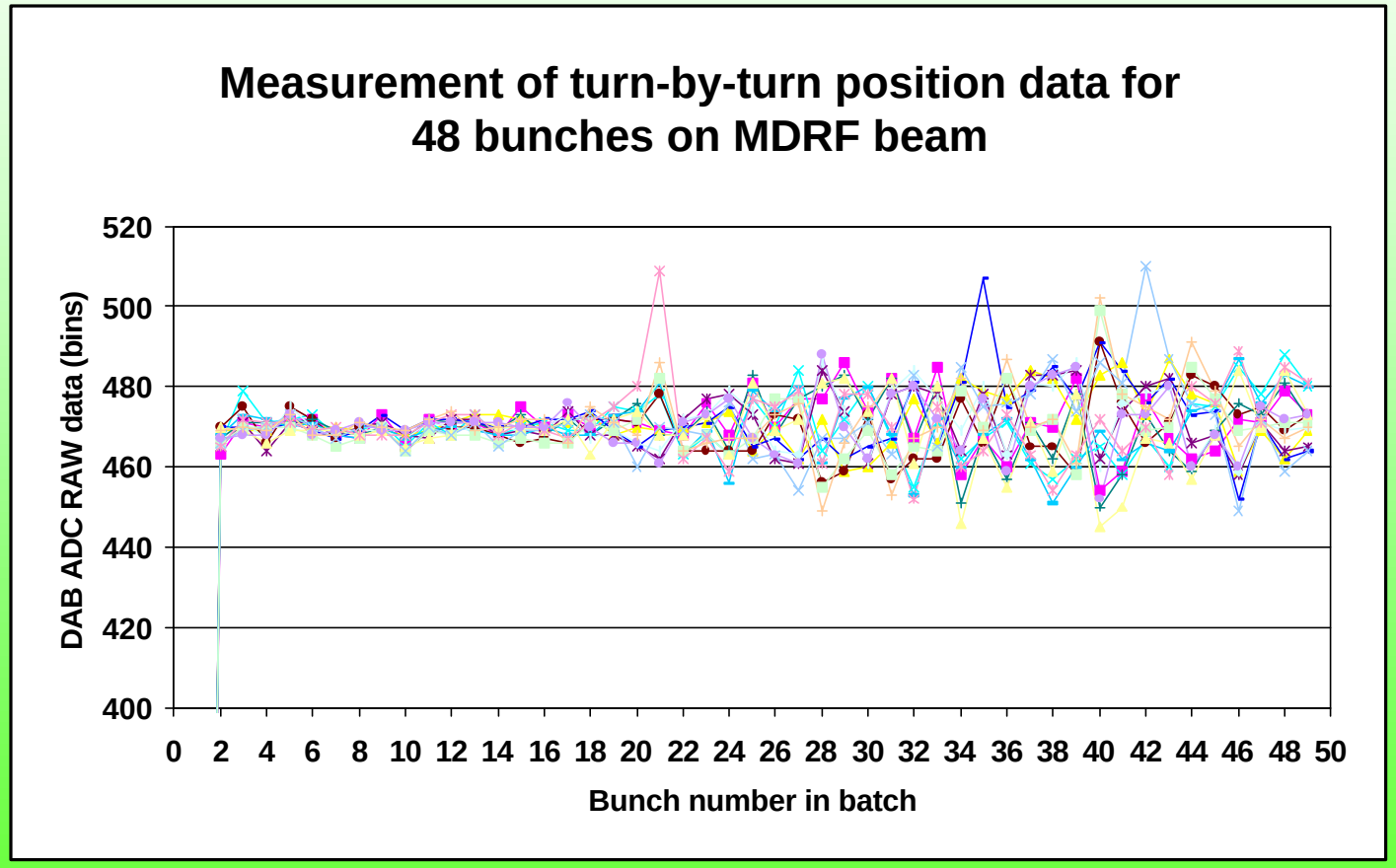
- **Calibration with MOPOS system Vertical plane**



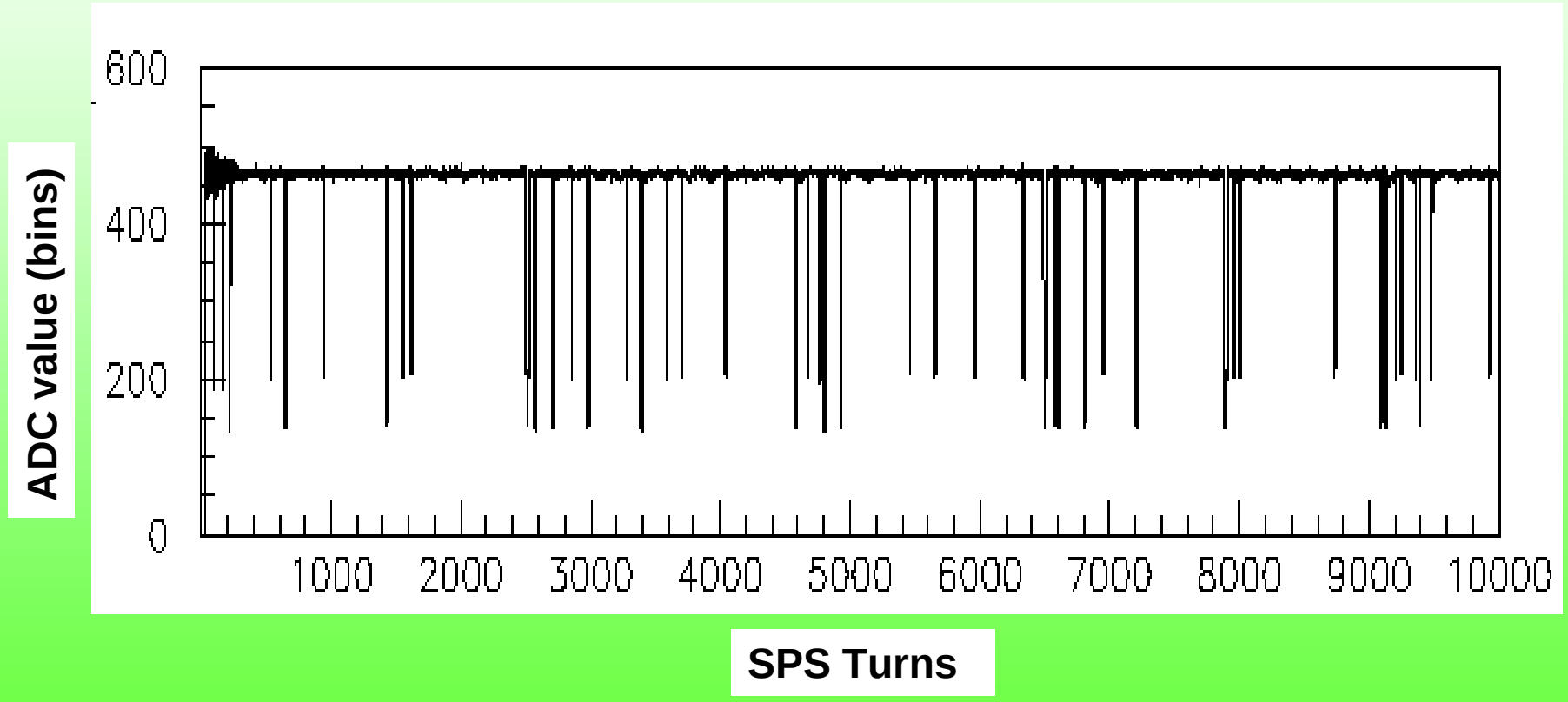
Measurements on the beam (AC dipole)



Measurements on the beam (Electron Cloud studies)

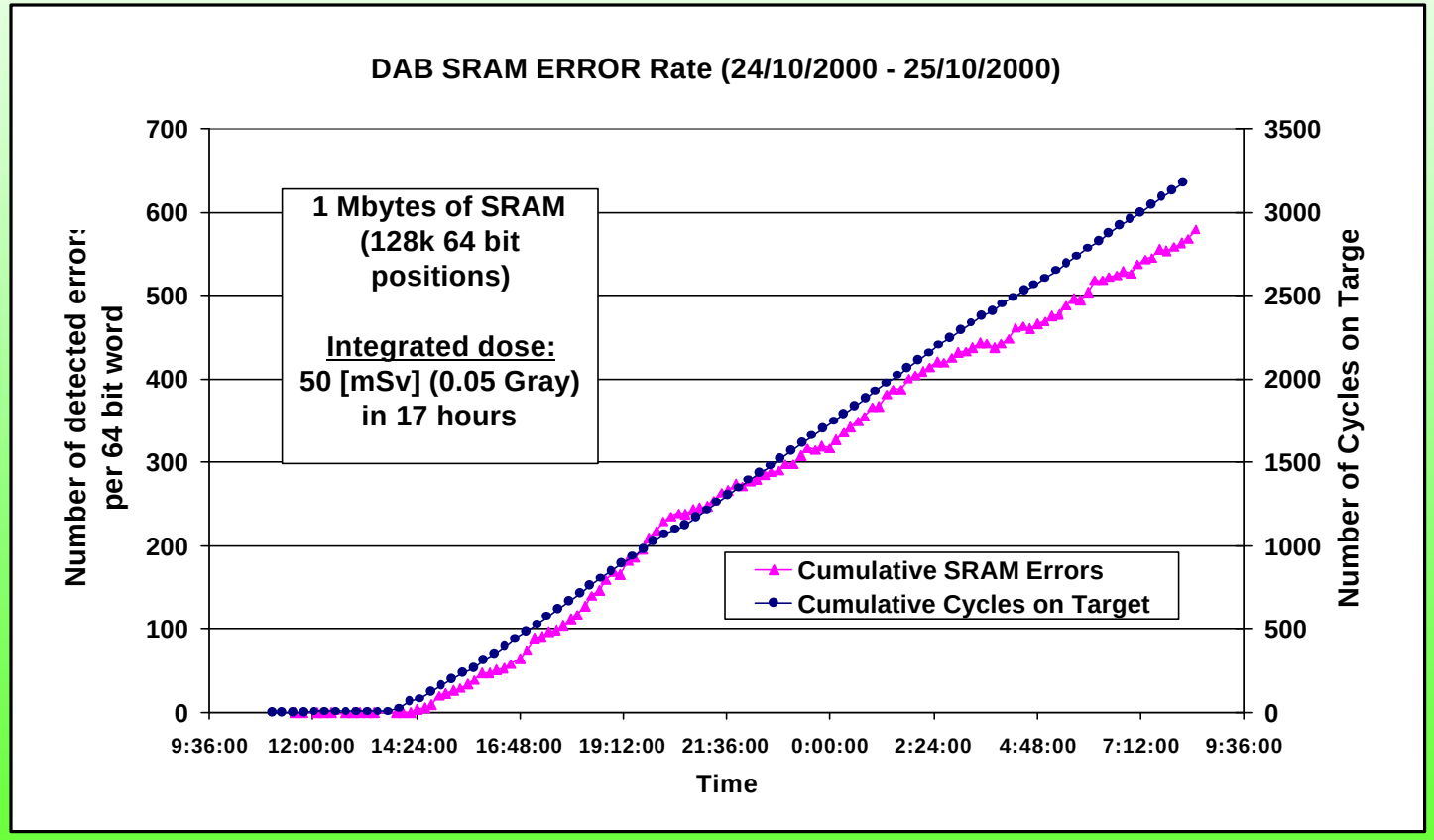


Cabling problems to WBTN in the vertical plane



Radiation tests TCC2

- **FPGA writes a known pattern to SRAM at reset and checks subsequently the content -> Error detection**



Future of the DAB module (SPS and LHC)

- **SPS replacement for IBMS (Ana)**
  - Beam intensity (FBCT) and position (based on WBTN) for individual LHC bunches
  - New front-end hardware development during 2001
  - Prototype system during 2002 in BA3
- **LHC Closed Orbit system**
  - CPU and DAB modules no-longer in LHC tunnel
  - Signals from WBTN transferred via optical fibre to surface buildings with easy access to VME crates in case of problems and no radiation (SRAM)

Conclusions

- The development of the DAB module (hardware and software) on the other side of the Atlantic has been a challenge in terms of communication
- Emails cannot replace face to face contact
- The DAB module has helped us to understand possible problems with the LHC Closed-Orbit system (radiation, cabling etc)
- Next generation of WBTN and DAB for LHC are being specified (dead-line February 2001). We hope that they will be based on an optical transmission of analogue signals